ANALOG DEVICES

Advanced Video Decoder with 10-Bit ADC, 3-Line Adaptive Comb Filter & Scaler

Preliminary Information

ADV7185

FEATURES

- Analog Video to Digital YUV Video Decoder
  - NTSC-(M/N), PAL-(B/D/G/H/I/M/N)
- Integrates Two 10-Bit Accurate ADCs
- Clocked from a Single 27 MHz Crystal
- Dual Video Clocking Schemes
  - Line Locked Clock Compatible (LLC)
  - Fixed Frequency Oversamping 10-Bit Operation
- Adaptive-Digital-Line-Length-Tracking (ADLLT™)
- Real Time Clock & Status Information Output
- Integrated AGC (Automatic Gain Control) & Clamping
- Simplified Digital Interface
- On-Board Digital FIFO
- Optimised Programmable Video Source Modes
  - Broadcast TV
  - VCR/Camcorder
  - Security/Surveillance
- Multiple, Programmable Analog Input Formats:
  - CVBS (Composite Video)
  - YUV and SVHS (Y/C) (Component Video)
- 6 Analog Input Video Channels
- Real Time Horizontal and Vertical Scaling
- Adaptive 3-Line Luma and Chroma Comb Filter
- Automatic NTSC/PAL Identification
- Differential Mode Video Input
- Digital Output Formats (20-Bit Wide Bus):
  - YCrCb (4:2:2 or 4:1:1)
  - CCIR601/CCIR656 8-Bit or Extended 10-Bit
- 0.5V to 2.0V pk-pk i/p range
- Differential Gain < 1%
- Differential Phase < 1°
- Programmable Video Controls
  - Pk-White/Hue/Brightness/Saturation/Contrast
- CCIR/Square Pixel Operation
- Integrated On-Chip Video Timing Generator
- Synchronous or Asynchronous Output Timing
- Line Locked Clock Output
- Close Captioning Passthrough Operation
- Vertical Blanking Interval Support
- Power Down Mode
- 2-Wire Serial MPU Interface (I^2C Compatible)
- +5V/+3V CMOS Supply Operation
- 80-Pin LQFP Package

APPLICATIONS

- Video Conferencing
- Hybrid Analog/Digital Set Top Boxes
- PC Video/Multimedia
- Professional Studio Quality Video
- Camcorders
- Security Systems/Surveillance

GENERAL DESCRIPTION

The ADV7185 is an integrated video decoder that automatically recognises and converts a standard analog baseband television signal compatible with world wide standards NTSC or PAL into 4:2:2 or 4:1:1 component video data compatible with 16-bit/8-Bit CCIR601/ CCIR656 8-Bit or 10-bit extended standards.

The advanced and highly flexible digital output interface enables perfomance video decoding and conversion in both frame-buffer based and line locked clock based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics including tape based sources, broadcast sources, secruity/surveillance cameras and professional systems.

Fully integrated line stores enable 3-line comb filtering in both luminance and chrominance data paths, plus real time horizontal and vertical scaling of captured video down to icon size. The 10-bit accurate A/D conversion provides professional quality SNR performance. This allows true 8-bit resolution in the 8-bit output mode and broadcast quality in 10-bit extended mode.
The 6 analog inputs channel accept standard composite or advanced component video including S-Video and YUV video signals in an extensive number of combinations. AGC and Clamp Restore circuitry allow an input video signal peak to peak range of 0.5V up to 2V. Alternatively these can be bypassed for manual settings.

The fixed 27 MHz clocking of the ADCs and datapath for all modes allows very precise and accurate sampling and digital filtering. The Line Locked Clock output allows the output data rate, timing signals and output clock signals to be synchronous, asynchronous or line locked even with +/-5% line length variation. The output control signals allow glueless interface connection in almost any application.

The ADV7185 modes are set up over a two wire serial bidirectional port (I^2C compatible).

The ADV7185 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7185 is packaged in a small 80 pin LQFP package.

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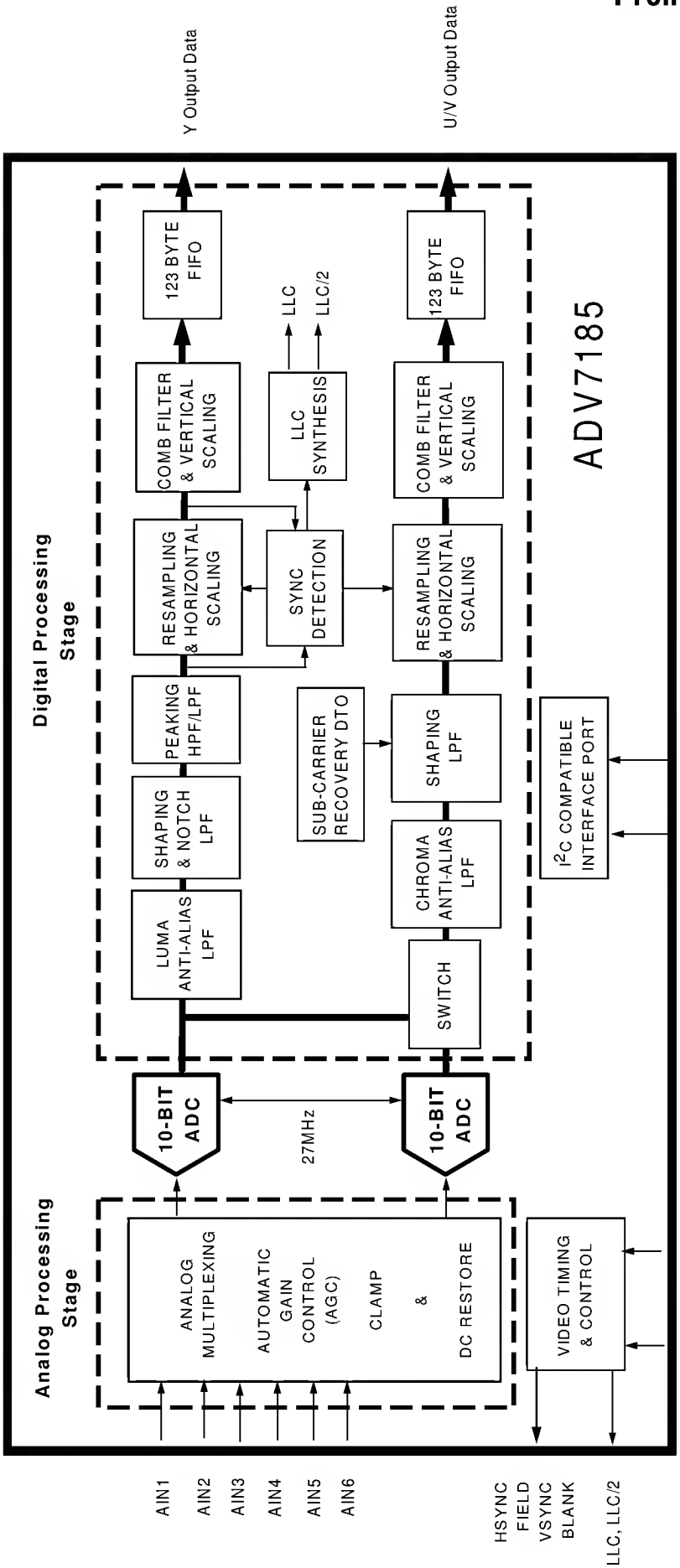


FUNCTIONAL BLOCK DIAGRAM

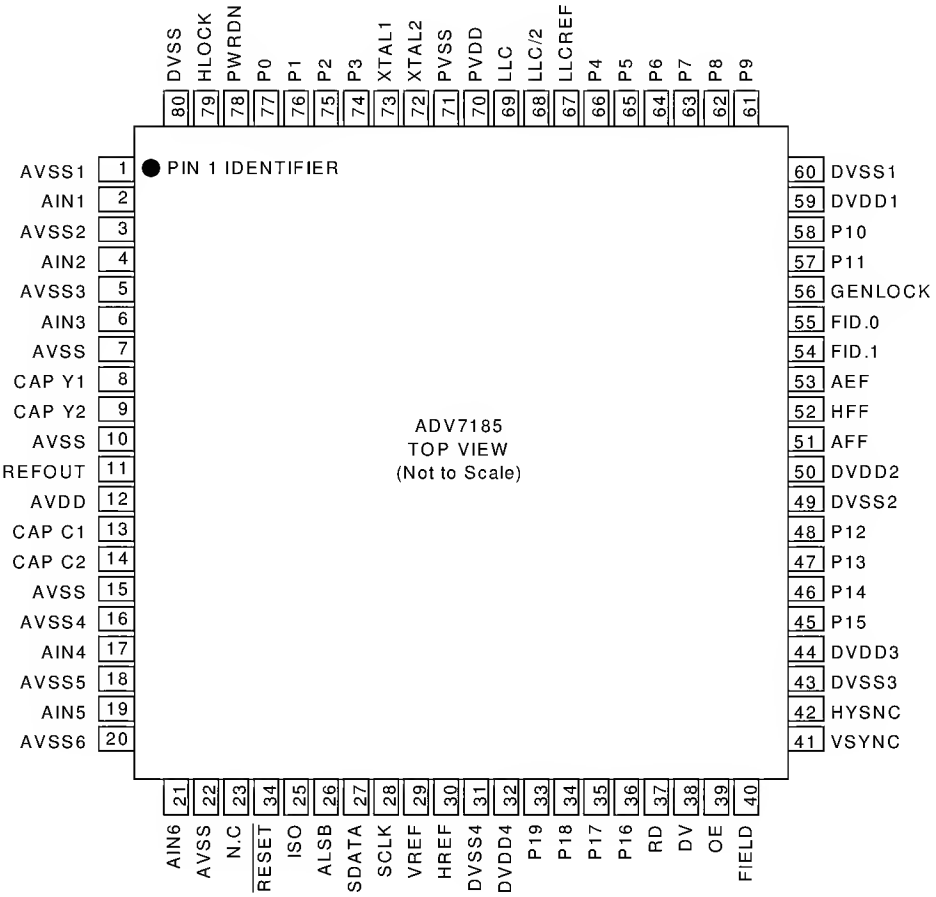
PIN DESCRIPTION

Mnemonic	Input/Output	Function
P19-P0	I	8-Bit Multiplexed YCrCb Pixel Port (P7-P0), 16-Bit YCrCb Pixel Port (P15-P0), 10-Bit Multiplexed Extended YCbCr Pixel Port (P9-P0) and 20-Bit YCbCr Pixel Port (P19-P0), P0 represents the LSB.
XTAL1	I	Input terminal for 27MHz crystal oscillator or connection for external oscillator with CMOS compatible square wave clock signal
XTAL2	O	Second terminal of crystal oscillator; not connected if external clock source is used
DVSS1-4	G	Ground for Digital supply
DVDD1-4	P	Digital Supply Voltage (5.0V)
AVSS	G	Ground for Analog Supply
AVDD	P	Analog Supply Voltage (5.0V)
AVDD1-3	P	Analog Input Channel supply Voltage (5.0)
AVSS1-4	G	Analog Input Channels ground
PVSS	G	PLL Supply Ground
PVDD	P	PLL Supply Voltage (5.0)
AIN1-6	I	Video Analog Input Channels
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal set up the LSB of the MPU address.
RD	I	Read signal, read data from FIFO
DV	O	Data Valid signal, indicates data on pixel port is a valid sample
OE	I	Output Enable, enables pixel port outputs or else tri-states them
HREF	O	Horizontal reference output signal (enable via I2C); this signal is used to indicate data on the YUV output. The positive slope indicates the begining of a new active line, HREF is always 720 Y samples long
VREF	O	Vertical reference output signal or inverse composite blanking signal depending on configuration
LLCREF	O	Clock reference ouput; this is a clock qualifier distributed by the internal CGC for a data rate of LLC2
LLC1	O	Line locked clock system output clock (27MHz)
LLC2	O	Line locked clock system output clock/2 (13.5MHz)
HLOCK	O	Horizontal locked: output signal indicating horizontal locking status
$\overline{\text{RESET}}$	I/O	System Reset, can be configured as an Input or Output signal.

PIN DESCRIPTION

Mnemonic	Input/Output	Function
PWRDN	I	Power down enable; place part in a power down status
REFOUT	O	Internal Reference Output
FID0-1	O	Field Indentification bits
AEF	O	Almost Empty Flag; FIFO control signal
HFF	O	Half Full Flag; FIFO control signal
AFF	O	Almost Full Flag; FIFO control signal
GENLOCK	O	Real Time Control Output; contains information for locking subcarrier frequency and phase locking
FIELD	O	ODD/EVEN field output signal
HSYNC	O	Horizontal sync output signal
VSYNC	O	Vertical sync output signal
ISO	I	Fast switch over I/P. allows the fast switch of video I/P channels
CAPY1-2	I	ADC Capacitor network
CAPC1-2	I	ADC Capacitor network

ADV7185 PIN FUNCTIONALITY



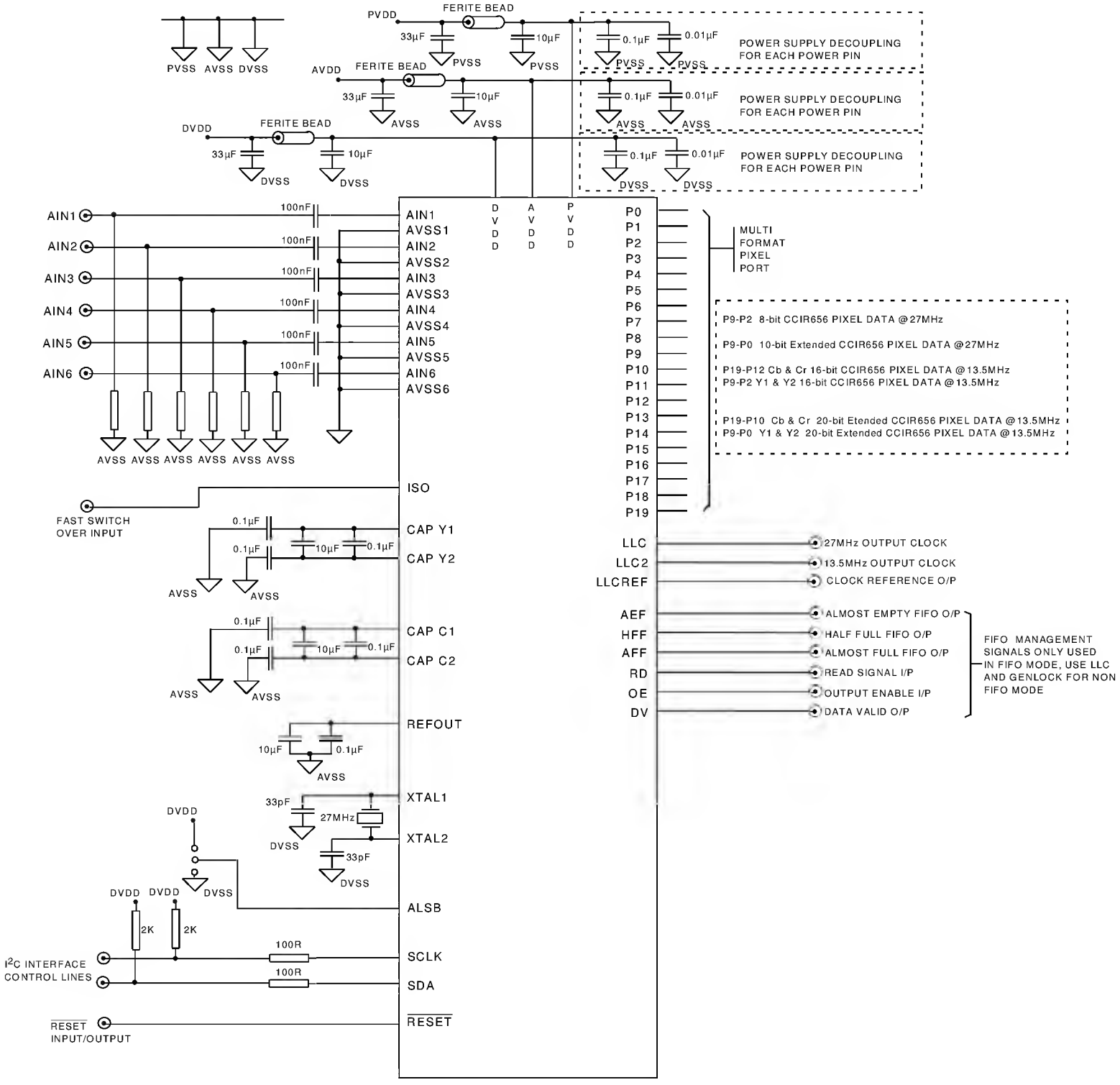


Figure 1. Recommended Circuit Layout

5V SPECIFICATIONS[1]

(V_{AA} = + 5V ± 5%, V_{DD} = + 5V ± 5%, All specifications T_{MIN} to T_{MAX} [2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (each ADC)			10	Bits	
Accuracy (each ADC)					
Integral Nonlinearity		±1.0		LSB	
Differential Nonlinearity		±0.5		LSB	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}	-1.0		1.0	µA	
Input Capacitance, C_{IN}			10	pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 3.2 mA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 0.4 mA
High Impedance Leakage Current			10	µA	
Output Capacitance			30	pF	
POWER REQUIREMENTS					
Digital Power Supply, V_{DD}	4.75	5.0	5.25	V	
Analog Power Supply, V_{AA}	4.75	5.0	5.25	V	
Digital Supply Current, I_{DD}			110	mA	YUV, square pixel,V_{DD}=5.25V
Analog Supply Current, I_{AA}			75	mA	YUV, square pixel,V_{AA}= 5.25V
Power-up Time		1		field	Sleep mode until powered up
AGC LOOP					
Time Constant		tbd		lines	TV mode: Sync depth variation until settled
Time Constant		tbd		lines	Surveillance mode: White peak violation until settled

NOTE

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range

[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.

Specifications subject to change without notice.

5V VIDEO PERFORMANCE SPECIFICATIONS[1]

(V_{AA} = + 5V ± 5%, V_{DD} = + 5V ± 5%, All specifications T_{MIN} to T_{MAX} [2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
NON-LINEAR SPECIFICATIONS					
Differential Phase		1		deg	CVBS, Comb/No Comb
Differential Gain		1		%	CVBS, Comb/No Comb
Luma Non-Linearity		1		%	
Chroma Non-Linear Gain		1		%	
NOISE SPECIFICATIONS					
SNR (Pedestal)		70		dB	CVBS
SNR (Ramp)		62		dB	CVBS
Luma/Chroma Crosstalk		tbd		dB	CVBS
Chroma/Luma Crosstalk		tbd		dB	CVBS
Analog Front End Channel Crosstalk		tbd		dB	S-Video/ YUV, single ended
Analog Front End Channel Crosstalk		tbd		dB	S-Video/ YUV, differential ended
LOCK TIME AND JITTER SPECIFICATIONS					
Horizontal Lock Time		20	tbd	lines	TV / VCR mode
Horizontal Recovery Time		20	tbd	lines	
Horizontal Lock Range		±5		%	
Line Length Variation Over Field		±5		%	VCR mode/ Surveillance mode
Line Length Variation Over Field		±1		%	TV mode
HLock Lost Declared		10	tbd	HSync	TV mode, No. of missing HSyncs
HLock Lost Declared		30	tbd	HSync	VCR/Surveillance mode, No. of missing HSyncs
Vertical Lock Time		2	tbd	VSync	First Lock into video signal
VLock Lost Declared		1	tbd	VSync	All modes, No. of missing VSyncs
F_{SC} Subcarrier Lock Range		±400		Hz	NTSC/PAL
Color Lock Time			15	lines	HLock to Color Lock Time
Data Jitter Resampling		1		ns	
LLC Jitter		< 1	tbd	ns	LLC Clock Generator only
LLC Jitter		3	tbd	ns	VCR/Surveillance mode only
LLC Jitter		1	tbd	ns	TV mode
CHROMA SPECIFIC SPECIFICATIONS					
Hue Accuracy		1		deg	
Hue Range		tbd		deg	Hue Control Register
Color Saturation Accuracy		1		%	
Color Saturation Range		tbd		dB	Saturation Control Register
Color Gain Control Range		-6	18	dB	S-Video, YUV, Overall CGC Range(analog and digital)
Analog Color Gain Range		-6	6	dB	S-Video, YUV
Digital Color Gain Range		0	12	dB	CVBS, S-Video, YUV
LUMA SPECIFIC SPECIFICATIONS					
Luma Brightness Accuracy		tbd		%	Video Input Range = 1.0Vp-p
Luma Brightness Range		tbd		%	Brightness Control Register
Luma Contrast Accuracy		tbd		%	Video Input Range = 1.0Vp-p
Luma Contrast Range		tbd		%	Contrast Control Register

NOTE

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range

[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.

Specifications subject to change without notice.

5V TIMING SPECIFICATIONS[1]

(V_{AA} = + 5V ± 5%, V_{DD} = + 5V ± 5%,
All specifications T_{MIN} to T_{MAX} [2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
SYSTEM CLOCK AND CRYSTAL					
Nominal Frequency		27		MHz	
Free-Run Frequency Deviation	-50		50	ppm	
Free-Run Temperature	-20		20	ppm	Temperature in the operating range
I²C PORT					
SCL Clock Frequency	0		400	kHz	
SCL min pulse width high, t_1	0.6			µs	
SCL min pulse width low, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	
Setup time (Start Condition), t_4	0.6			µs	
Data Setup Time, t_5	100			ns	
SCL/SDA Rise Time, t_6			300	ns	
SCL/SDA Fall Time, t7			300	ns	
Setup Time (Stop Condition), t_8		0.6		µs	
RESET FEATURE					
Reset Pulse Input Width	tbd			µs	
Reset Pulse Output Width	tbd			µs	
CLOCK OUTPUTS					
LLC Cycle Time	33.8	37	40.7	ns	CCIR601 video, nominal line length and square pixel lenghts
LLC2 Cycle Time	67.6	74	81.4	ns	CCIR 601 video, nominal line length and square pixel lenghts
LLC to LLC2 Delay		1		ns	
LLC to Data Delay		tbd		ns	
LLC duty cycle	40	50	60	%	
LLC/LLC2 rise time			5	ns	
LLC/LLC2 fall time			5	ns	
DATA AND CONTROL OUTPUT					
Data Output Hold Time		tbd		ns	
Data Setup Time		tbd		ns	
Propagation Delay to HiZ		tbd		ns	

NOTE
[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range
[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
Specifications subject to change without notice.

5V ANALOG FRONT END SPECIFICATIONS[1]

(V_{AA} = + 5V ± 5%, V_{DD} = + 5V ± 5%, All specifications T_{MIN} to T_{MAX} [2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
PROGRAMMABLE GAIN AMPLIFIER					
Temperature Stability		0.2	tbd	%	Over temperature range
Supply Stability		0.2	tbd	%	Over V_{AA} range
Absolute Gain Variation		2	tbd	%	Dependent on process
Resolution		9	tbd	bits	Linear in dB
Gain Range Luma	-6		6	dB	
Gain Range Chroma	-6		6	dB	
Input Voltage Range	0.5	1.0	2.0	V	
CLAMP CIRCUITRY					
External Clamp Capacitor		0.1		µF	
Input Impedance		200		kΩ	Clamp switched off
Clamp Source Current		2		µA	Signal already clamped (fine clamping)
Clamp Sink Current		2		µA	Signal already clamped (fine clamping)
Clamp Source Current		tbd		mA	Aquire mode (fast clamping)
Clamp Sink Current		tbd		mA	Aquire mode (fast clamping)

NOTE

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range

[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.

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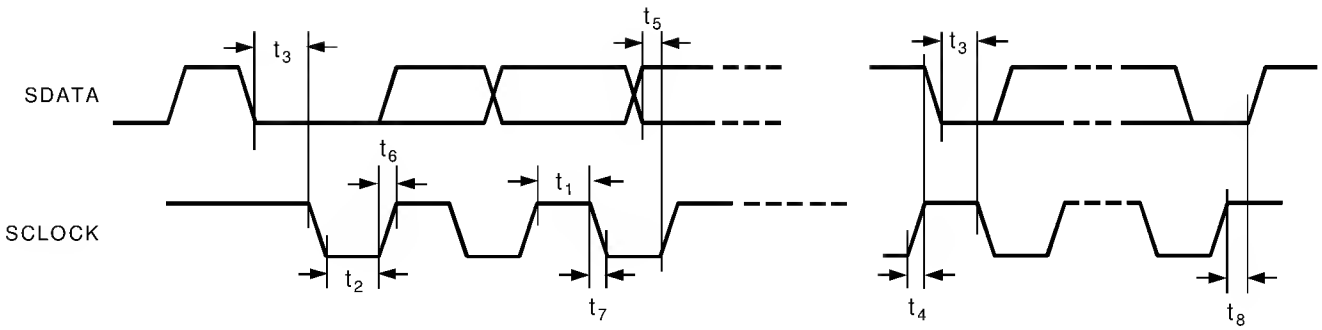

Figure 2. MPU Port Timing Diagram